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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,091	06/01/2001	Yasuteru Araya	14669	2464

23389 7590 07/12/2005

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EXAMINER	
THANGAVELU, KANDASAMY	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/872,091	ARAYA ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *May 3, 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to the Applicants' Amendment dated May 3, 2005. Claims 12, 15 and 16 were amended. Claims 11-19 of the application are pending. This office action is made non-final in response to the request for continued examination.

Information Disclosure Statement

2. Acknowledgment is made of the information disclosure statement filed on May 3, 2005. The paper provided with the information disclosure statement has been considered in reviewing the claims.

Drawings

3. In Figure 1, "structuring the simulation platform" appears to be incorrect and it appears that it should be "structuring the simulation program". Corrected drawing is required in reply to this office action.

Abstract

4. The abstract is objected to because of the following informalities:

In the amendments to the abstract sent on November 26, 2004, Line 7, "the sources are subjected to isolation of the hardware and software" is not understood. The specification does not state why hardware is isolated from the software.

Lines 8-9, "to count the bus traffic of the bus interconnecting between the hardware and software" appears to be incorrect and it appears that it should be "to count the bus traffic of the bus interconnecting the hardware and software".

Lines 10-12, "evaluation is performed on the performance of the bus, so that the bus traffic for its processing rate is to be finally produced" appears to be incorrect and it appears that it should be "evaluation is performed on the performance of the bus, so that the bus traffic for its processing rate is finally produced".

Lines 13-14, "such that isolation of the hardware and software is optimized in response to the bus traffic"". The specification does not state how the optimization is done.

Lines 15-16, "This brings exclusion of feedback loops derived from the cooperative verification after actual coding". The specification does not state why the feedback loops are excluded and how it is achieved.

Appropriate corrections are required.

Specification

5. The disclosure is objected to because of the following informalities:

In the amendments to the specification sent on May 3, 2005, in the paragraph beginning on Page 2, Line 3, "verification is made as to whether the sources operate correct or not" appears to be incorrect and it appears that it should be "verification is made as to whether the sources operate correctly or not".

Specification Page 1, Lines 20-21 state, "it is troublesome for manufacturers to perform verification on the systems by using the specially designed LSI devices". Why is it troublesome? Did the applicants meant to say, "it is expensive" or "it is time consuming"?

In specification Page 2, Line 2, "simulation platform" should be "simulation program".

In specification Page 2, Lines 5-6 " simulation platform" should be "simulation program".

Specification Page 2, Lines 5-6 state, "isolation of the hardware and software is performed on the structured simulation platforms, which are divided into hardware elements and software elements". This statement is not understood. Does the applicant refer to the hardware and software elements of the simulation platform?

In specification Page 2, Lines 17-18, "the procedures for the LSI design and development should meet some essential conditions raising the requirements of the system simulation" is not understood. What is raising the requirements of system simulation?

In specification Page 3, Lines 23-25, "to considerably reduce turnaround times in design of LSI by excluding unwanted operations regarding feedback loops" is not

understood. What are unwanted operations regarding feedback loops? How are they excluded? They are excluded from what?

In specification Page 4, Lines 2-3, "isolation of the hardware and software being effected with respect to the sources described" is not understood. Why is software isolated from hardware? Which software is isolated from which hardware? What does "being effected with respect to the sources" mean?

Specification Page 4, Lines 8-10 state, "the isolation of the hardware and software is optimally performed at the prescribed stage of the architecture design". How is this optimization done and what is the objective function optimized?

In specification Page 4, Lines 11-12, "exclude the feedback loops regarding the isolation between the hardware and software from the cooperative verification" is not understood. What are feedback loops regarding the isolation between the hardware and software?

In specification Page 4, Line 22, "the bus interconnecting between the hardware and software" appears to be incorrect and it appears that it should be "the bus interconnecting the hardware and software".

Specification Page 5, Line 2 states, "isolation of the hardware and software is optimized in response to the bus traffic". How is this optimization done and what objective function is optimized?

In specification Page 5, Lines 3-5, "exclusion of the feedback loops derived from the cooperative verification" is not understood. What are feedback loops derived from the cooperative verification and how are they excluded? They are excluded from what?

In specification Page 6, Line 24, " simulation platform" should be "simulation program".

Specification Page 7, Lines 1-2 state, "the evaluation function has an operation of counting a certain value". What is the "certain value" being counted?

In specification Page 7, Lines 3-4, "the bus interconnecting between the hardware and software" appears to be incorrect and it appears that it should be "the bus interconnecting the hardware and software".

Specification Page 7, Lines 5-6 state, "sources that are used in the algorithm design are modified by executing the created evaluation function". Does this mean that the created evaluated function is executed and it modifies the sources?

Specification Page 7, Line 16 states, "processing rate requested by a main function is provided". What is this processing rate requested by the main function? Is it the CPU speed or instructions per second? Or is it the bus operating speed?

In specification Page 7, Line 20, "check the validity with respect to isolation of the hardware and software" is not understood. How is the validity checked? What is the process used for validity checking?

Specification Page 7, Line 21 states, "if validity check causes a change of bus". How does the validity check cause a change of bus? What is change of bus? Does it mean the bus width or capacity is changed?

Specification Page 8, Lines 12-13 state, "cooperative verification is performed on unification of the hardware and software". What is unification of hardware and software?

In specification Page 9, Lines 19-20, "to change the bus interconnecting between the hardware and software" appears to be incorrect and it appears that it should be "to change the bus interconnecting the hardware and software".

In specification Page 9, Line 22 " simulation platform" should be "simulation program".

In specification Page 10, Lines 9-10, "so that evaluation is to be performed on the performance of the bus" appears to be incorrect and it appears that it should be "so that evaluation is performed on the performance of the bus".

Specification Page 10, Lines 19-20 state, "the evaluation function meets the operation of incrementing a certain value". What is the "certain value" being incremented?

In specification Page 16, Line 2 " simulation platform" should be "simulation program".

Specification Page 18, Lines 23-24 state, "by executing a specific evaluation function for increment by a certain value". What is the "certain value" being incremented?

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. §112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 11-19 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In the paragraphs below, ***new material*** refers to the material added in the amendment of November 26, 2004.

7.1 Claim 11, Lines 5-7 state, "structuring source code describing the algorithm design in a general purpose high-level programming language by isolating elements of said source code representing hardware units and software units" and Lines 13-14 state, "performing said performance evaluation by simulating said modified source code elements and evaluating said data transfer on the bus".

Specification Page 2, Lines 1-7 state, "Prior to actual manufacturing, simulation programs (or algorithms) are normally structured without consideration of distinctions between hardware and software... Next, isolation of hardware and software is performed on the structured simulation programs, which are divided into hardware elements and software elements respectively. The isolation of hardware and software is made by experiments".

It is not understood as to what is meant by "isolation of hardware and software is performed on the structured simulation programs". Are the simulation programs or simulation platforms divided into hardware and software elements?

Specification Page 6, Lines 22-25 state, "a simulation program is structured to perform architecture design by using sources ...in simulation program structuring process, the flow proceeds to step A3 to effect isolation of hardware and software". Therefore it is understood that structuring the simulation program involves isolation of the hardware and software.

The simulation program is a software tool and it is not hardware. Therefore the structuring of simulation platform involving ***isolation of hardware and software*** mentioned in Specification, Page 6, Lines 22-25 is not understood.

One of ordinary skill in the art will understand that bus operations involve both bus hardware and bus operational software. There is much interaction between hardware and software. Any simulation model of the bus operation will involve both the hardware models and the software models. Therefore it is not understood as to why one will isolate hardware and software in any simulation model of bus operations and how it will affect the simulated bus performance.

It is also not understood as to how "The isolation of hardware and software is made by experiments". The specification does not state as to what criteria and process are used to isolate the hardware and software during structuring the simulation program. Therefore the process of structuring the simulation program is not properly described in the specification.

In view of the lack of proper description of the structuring process in the specification, "structuring source code describing the algorithm design in a general purpose high-level

programming language by isolating elements of said source code representing hardware units and software units" is not understood.

In addition, the statement, "isolating elements of said source code representing hardware units and software units" is ***new material*** not found in the original specification and therefore this amendment to the claim is not allowed.

7.2 Claim 11, Lines 11-12 state, "modifying at least one element of said source code elements based on a ***result*** of an implementation of said evaluation function". The specification does not describe ***the result*** of implementation of the evaluation function. This is ***new material*** not found in the original specification and therefore this amendment to the claim is not allowed.

7.3 Claim 11, Lines 13-14 state, "performing said performance evaluation by simulating said modified source code elements and evaluating said data transfer on the bus". What is ***evaluating data transfer***? Does it mean the number of bytes transferred or the quality of the data received at the destination? The specification does not describe ***evaluating the data transfer*** on the bus. It states on Page 4, Lines 24-25, "evaluation is performed on the performance of the bus, so that the ***bus traffic*** for the processing rate is finally produced". Page 7, Lines 1-2 state, "the evaluation function has an operation of counting a certain value". Fig. 2 shows that the evaluation function increments a counter by 1, each time a data is written. Therefore there is no support for "evaluating said data transfer on the bus". This is ***new material*** not found in the original specification and therefore this amendment to the claim is not allowed.

7.4 Claim 12, Line 2 states, "restructuring the source code based on the evaluated data transfer". The specification does not describe ***evaluating the data transfer*** as explained in Paragraph 7.3 above. This is ***new material*** not found in the original specification and therefore this amendment to the claim is not allowed.

7.5 Claim 12 refers to, "restructuring the source code based on the evaluated data transfer; and performing said performance evaluation again by simulating said restructured source code again". The process of structuring the source code is not properly described in the specification, as explained in Paragraph 7.1 above. The term ***evaluating data transfer*** is ***new material*** as described in Paragraph 7.3 above.

7.6 Claim 13, Lines 1-2 state, "a bus traffic is calculated from the evaluated data transfer with respect to the processing rate of the bus". The specification does not describe evaluating the data transfer as explained in Paragraph 7.3 above. This is ***new material*** not found in the original specification and therefore this amendment to the claim is not allowed.

7.7 Claim 14 refers to, "feeding back a result of the performance evaluation of the bus to the step of structuring the source code to improve the architecture design at a high-level design stage by isolating in said source code new elements representing hardware units and new elements representing software units". The process of structuring the source code is not properly described in the specification, as explained in Paragraph 7.1 above.

In addition, the statement, "isolating in said source code new elements representing hardware units and new elements representing software units" is ***new material*** not found in the original specification and therefore this amendment to the claim is not allowed.

7.8 Claim 15 refers to "isolation of the source code into elements representing hardware units and elements representing software units". This is ***new material*** not found in the original specification and therefore this amendment to the claim is not allowed.

7.9 Claim 16, Lines 12-14 refer to, "structuring the source code into elements representing at least one of the hardware units and the software units for use in the architecture design by compiling said structured source code elements". The process of structuring the source code is not properly described in the specification, as explained in Paragraph 7.1 above.

In addition, the statement, "into elements representing at least one of the hardware units and the software units" is ***new material*** not found in the original specification and therefore this amendment to the claim is not allowed.

7.10 Claims rejected but not specifically addressed are rejected based on their dependency on rejected claims.

8. Claim 15 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

8.1 Claim 15 states, "in response to the bus traffic, isolation of the source code into elements representing hardware units and elements representing software units is optimized". The specification does not describe anywhere how this isolation of the source code in elements representing hardware units and elements representing software units is optimized. It does not describe the objective function and the process used for optimization of isolation of the source code into elements representing hardware units and elements representing software.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16, Lines 12-14 state, "structuring the source code into elements representing at least one of the hardware units and the software units for use in the architecture design by compiling said structured source code elements".

The claim is thus circular because structuring the source code into elements representing at least one of the hardware units and the software units is done by compiling said structured source code elements, thus making the claim indefinite.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 11-15 and 17-19 are rejected under 35 U.S.C. 102(a) and 102(b) as being anticipated by **Tammemae et al.** ("AKKA: A tool for cosynthesis and prototyping", The Institution of Electrical Engineers, UK, 1996).

12.1 **Tammemae et al.** teaches AKKA: A tool for cosynthesis and prototyping. Specifically, as per claim 11, **Tammemae et al.** teaches a method in a LSI design and development process (Page 1, Para 1, L1-2; Page 1, Para 2, L2-5), for evaluating an architecture design for an algorithm design by performing a performance evaluation of at least one bus at a high-level stage of the design and development process (Page 1, Para 2, L2-4; Page 1, Para 4, L2; Page 2, Para 4, L3); the method comprising:

structuring source code describing the algorithm design in a general purpose high-level programming language (Page 1, Para 2, L2-3; Page 1, Para 3, L1-3), by isolating elements of the

source code representing hardware units and software units (Page 1, Para 2, L3; Page 1, Para 3, L7-8; Page 3, Fig. 1);

creating an evaluation function for evaluating data transfer that occurs on the at least one bus (Page 1, Para 4, L2; Page 1, Para 2, L3-4; Page 2, Para 4, L3; Page 3, Fig. 1; Page 2, Para 2, L4), the bus being a part of the source code realizing the data transfer between the elements representing hardware units and software units (Page 1, Para 4, L2; Page 1, Para 2, L3-4; Page 1, Para 5, L5-6; Page 2, Para 2, L4);

modifying at least one element of the source code elements based on a result of an implementation of the evaluation function (Page 2, Para 5, L1-3; Page 2, Para 4, L3; Page 2, Para 2, L4); and

performing the performance evaluation by simulating the modified source code elements and evaluating the data transfer on the bus (Page 2, Para 5, L1-3; Page 3, Fig. 1; Page 4, Para 1, L2-3).

Per claim 12: **Tammemae et al.** teaches restructuring the source code based on the evaluated data transfer (Page 1, Para 2, L3-4; Page 1, Para 4, L1-2); and

performing the performance evaluation again by simulating the restructured source code again (Page 2, Para 5, L1-3; Page 3, Fig. 1; Page 4, Para 1).

Per claim 13: **Tammemae et al.** teaches that a bus traffic is calculated from the evaluated data transfer with respect to the processing rate of the bus (Page 2, Para 5, L1-3).

Per claim 14: **Tammemae et al.** teaches feeding back a result of the performance evaluation of the bus to the step of structuring the source code to improve the architecture design at a high-level design stage by isolating in the source code new elements representing hardware units and new elements representing software units (Page 1, Para 2, L3-4; Page 1, Para 4, L1-2; Page 2, Para 5, L1-3).

Per claim 15: **Tammemae et al..** teaches that in response to the bus traffic, isolation of the source code into elements representing hardware units and elements representing software units is optimized (Page 1, Para 2, L3-4; Page 1, Para 4, L1-2; Page 2, Para 5, L1-3).

Per claim 17: **Tammemae et al.** teaches that the variables loaded onto the bus consist of n bits while the bus consists of m bit lines, where n and m are both integers, and n is a multiple of m, and the bus traffic for the processing rate is produced such that the number of times in effecting data transfer on the bus is multiplied by n/m and is then divided by the processing rate (Page 2, Para 5, L1-3). **Tammemae et al.** teaches that each variable access is counted using a counter and a log of the access of the variables is made. It is inherent that from the counting of the variable access to a bus, and the log of the variable accesses, it is possible to calculate the number of times the bus was used if the bus width was smaller than the variable length requiring multiple accesses to the bus for each variable loaded onto the bus.

Per claim 18: **Tammemae et al.** teaches that the general purpose high-level language is one of C language and C++ language (Page 1, Para 2, L2-3; Page 1, Para 3, L1-3).

Per claim 19: **Tammemae et al.** teaches that the evaluation function increments a counting value if a pre-defined variable is loaded onto the bus (Page 2, Para 5, L1).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

14. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

15. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Tammemae et al.** ("AKKA: A tool for cosynthesis and prototyping", The Institution of Electrical Engineers, UK, 1996) in view of **Raimi et al.** (U.S. Patent 5,604,895) and **Adams et al.** ("Execution time profiling for multiple process behavioral synthesis", IEEE, 1995).

15.1 As per claim 16, **Tammemae et al.** teach the method of claim 11. **Tammemae et al.** teaches creating the evaluation function (Page 1, Para 4, L2; Page 1, Para 2, L3-4; Page 2, Para 4, L3; Page 3, Fig. 1; Page 2, Para 2, L4);

profiling the source code based on whether a line of source code represents writing data to variables that are defined in advance and are loaded onto the bus to be evaluated (Page 2, Para 4, L3; Page 2, Para 2, L4);

structuring the source code into elements representing at least one of the hardware units and the software units for use in the architecture design by compiling the structured source code elements (Page 1, Para 2, L3; Page 1, Para 3, L7-8; Page 3, Fig. 1);

calculating the data transfer rate on the bus by executing the compiled source code elements in a simulation program (Page 2, Para 5, L1-3; Page 3, Fig. 1; Page 4, Para 1, L2-3);

calculating bus traffic with regard to a given processing rate of the bus (Page 2, Para 5, L1-3); and

performing evaluation of the performance of the bus in response to the bus traffic (Page 2, Para 5, L1-3; Page 3, Fig. 1; Page 4, Para 1, L2-3).

Tammemae et al. does not expressly teach after creating the evaluation function, sequentially reading in the source code line by line while effecting syntax analysis; determining whether the source code is to be modified based on whether a line of source code represents writing data to variables that are defined in advance and are loaded onto the bus to be evaluated; upon determining that the source code is to be modified, modifying the source code by

embedding the evaluation function one of immediately before or immediately after the line of source code in which the variable is written; and repeating the forgoing steps until the source code is completely read in up to a last line of source code. **Raimi et al.** teaches after creating the evaluation function, sequentially reading in the source code line by line while effecting syntax analysis (Abstract, L5-6; CL2, L20-22); determining whether the source code is to be modified based on whether a line of source code represents writing data to variables that are defined in advance and are loaded onto the bus to be evaluated (CL1, L26-32; CL1, L64-66; CL2, L37-54); upon determining that the source code is to be modified, modifying the source code by embedding the evaluation function one of immediately before or immediately after the line of source code in which the variable is written (CL1, L26-32; CL1, L64-66; CL2, L23-29; CL2, L37-54); and repeating the forgoing steps until the source code is completely read in up to a last line of source code (Abstract, L5-6; CL2, L20-22), because that allows generation of additional code to check for the occurrence of bus access events (CL1, L65-66). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Tammemae et al.** with the method of **Raimi et al.** that included after creating the evaluation function, sequentially reading in the source code line by line while effecting syntax analysis; determining whether the source code was to be modified based on whether a line of source code represented writing data to variables that were defined in advance and were loaded onto the bus to be evaluated; upon determining that the source code was to be modified, modifying the source code by embedding the evaluation function one of immediately before or immediately after the line of source code in which the variable was written; and repeating the forgoing steps until the source code was completely read in up to a last line of source code. The

artisan would have been motivated because that would allow generation of additional code to check for the occurrence of bus access events.

In addition, **Adams et al.** teaches after creating the evaluation function, sequentially reading in the source code line by line while effecting syntax analysis; determining whether the source code is to be modified based on whether a line of source code represents writing data to variables that are defined in advance and are loaded onto the bus to be evaluated; upon determining that the source code is to be modified, modifying the source code by embedding the evaluation function one of immediately before or immediately after the line of source code in which the variable is written; and repeating the forgoing steps until the source code is completely read in up to a last line of source code (Page 144, Fig. 1; Abstract, L1-3; Page 145, CL1, Para 2), because that results in a simulation model that has the same cycle-by-cycle behavior as the RTL model but can be simulated in a fraction of the time (Abstract, L4-6); it allows performance of the system to evaluated dynamically, by simulating the system, using a simulation model that accurately reflects the results of behavioral synthesis (Page 144, CL1, Para 3, L7-10).

Response to Arguments

16. Applicants' arguments with respect to 35 USC 112 first Paragraph and 35 USC 103 (a) rejections filed on April 21, 2005 have been considered. Applicants' arguments with respect to 35 USC 112 first Paragraph and 35 USC 103 (a) rejections are not persuasive.

16.1 As per the applicants' argument that "the isolation of the software and the hardware features in the claims, and the evaluation process using the bus features, are fully supported by the original Specification; further, the claims will be readily understood by a person of ordinary skill in the art in the light of Applicant's original Disclosure", the Examiner respectfully disagrees.

Specification Page 2, Lines 1-7 state, "Prior to actual manufacturing, simulation programs (or algorithms) are normally structured without consideration of distinctions between hardware and software... Next, isolation of hardware and software is performed on the structured simulation programs, which are divided into hardware elements and software elements respectively. The isolation of hardware and software is made by experiments".

It is not understood as to what is meant by "isolation of hardware and software is performed on the structured simulation programs". Are the simulation programs or simulation platforms divided into hardware and software elements?

Specification Page 6, Lines 22-25 state, "a simulation program is structured to perform architecture design by using sources ...in simulation program structuring process, the flow proceeds to step A3 to effect isolation of hardware and software". Therefore it is understood that structuring the simulation program involves isolation of the hardware and software.

The simulation program is a software tool and it is not hardware. Therefore the structuring of simulation platform involving ***isolation of hardware and software*** mentioned in Specification, Page 6, Lines 22-25 is not understood.

One of ordinary skill in the art will understand that bus operations involve both bus hardware and bus operational software. There is much interaction between hardware and

software. Any simulation model of the bus operation will involve both the hardware models and the software models. Therefore it is not understood as to why one will isolate hardware and software in any simulation model of bus operations and how it will affect the simulated bus performance.

It is also not understood as to how "The isolation of hardware and software is made by experiments". The specification does not state as to what criteria and process are used to isolate the hardware and software during structuring the simulation program. Therefore the process of structuring the simulation program is not properly described in the specification.

In view of the lack of proper description of the structuring process in the specification, "structuring source code describing the algorithm design in a general purpose high-level programming language by isolating elements of said source code representing hardware units and software units" is not understood.

16.2 As per the applicants' argument that "Chang does not disclose or suggest isolating elements of the source code representing hardware units and software units, as required by independent claim 11; ... Chang is incapable of disclosing or suggesting modifying source code elements based on a result of implementation of the evaluation function, the evaluation function evaluating data transfer that occurs on the bus, as further required by independent claim 11; ...Tseng is related to a TIFG logic device, whereas the present invention teaches isolation of hardware and software; Swoboda teaches semiconductor chips and is related to LSI testing, and discloses methods to compile, assemble, and link software code; ... Swoboda teaches how to put algorithm design into the RTL description, which merely corresponds to the after-processing,

unlike with the present invention; Fujiwara is directed to chips and LSI, and discloses an implementation for putting the RTL description into the LSI; Chang and the other cited references, even if taken together in combination as a whole, do not disclose or suggest the recitations of independent claim 11", the Examiner has used a new reference **Tammemae et al.** ("AKKA: A tool for cosynthesis and prototyping", The Institution of Electrical Engineers, UK, 1996).

As per claim 11, **Tammemae et al.** teaches a method in a LSI design and development process (Page 1, Para 1, L1-2; Page 1, Para 2, L2-5), for evaluating an architecture design for an algorithm design by performing a performance evaluation of at least one bus at a high-level stage of the design and development process (Page 1, Para 2, L2-4; Page 1, Para 4, L2; Page 2, Para 4, L3); the method comprising:

structuring source code describing the algorithm design in a general purpose high-level programming language (Page 1, Para 2, L2-3; Page 1, Para 3, L1-3), by isolating elements of the source code representing hardware units and software units (Page 1, Para 2, L3; Page 1, Para 3, L7-8; Page 3, Fig. 1);

creating an evaluation function for evaluating data transfer that occurs on the at least one bus (Page 1, Para 4, L2; Page 1, Para 2, L3-4; Page 2, Para 4, L3; Page 3, Fig. 1; Page 2, Para 2, L4), the bus being a part of the source code realizing the data transfer between the elements representing hardware units and software units (Page 1, Para 4, L2; Page 1, Para 2, L3-4; Page 1, Para 5, L5-6; Page 2, Para 2, L4);

modifying at least one element of the source code elements based on a result of an implementation of the evaluation function (Page 2, Para 5, L1-3; Page 2, Para 4, L3; Page 2, Para 2, L4); and

performing the performance evaluation by simulating the modified source code elements and evaluating the data transfer on the bus (Page 2, Para 5, L1-3; Page 3, Fig. 1; Page 4, Para 1, L2-3).

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

The following patents are cited to further show the state of the art with respect to partitioning the architecture between hardware and software, profiling the software description to determine various events, and bus performance analysis using a set of hardware/software partitions selected.

1. Raghunathan et al., "System for the design of high performance communication architecture for system-on-chips using communication architecture tuners", U.S. Patent 6,694,488, February 2004.

2. Brage et al., "A codesign case study in computer graphics", IEEE, 1994.

3. Vahid et al., "Toward a model for hardware and software functional partitioning", IEEE, 1996.

4. Lahiri et al., " Fast performance analysis of bus-based system-on-chip communication architectures", IEEE, 1999.

5. Knudsen et al., " Integrating communication protocol selection with hardware/software codesign", IEEE, 1999.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard, can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

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you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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July 6, 2005